AMENDMENTS

In The Claims

1. (original) A thin film transistor, comprising:

a gate electrode, formed on a substrate, wherein the gate electrode has at least one notch;

a gate dielectric layer, formed over the substrate, covering the gate electrode;

a source region, formed on the gate dielectric layer, wherein the source region is located over a region outside the notch of the gate electrode and the source region overlaps a portion of the gate electrode;

a drain region, formed over the gate dielectric layer exposed by the source region, wherein the drain region is over the notch of the gate electrode and the drain region overlaps a portion of the gate electrode at the edge of the notch; and

a channel layer formed on the gate dielectric layer and located over the gate electrode and between the source region and drain region.

2. (original) The thin film transistor of claim 1, further comprising an etch stop layer formed between the channel layer and the source and drain regions.

3. (original) The thin film transistor of claim 1, further comprising an ohmic-contact layer formed between the channel layer and the source and drain regions.

4. (original) The thin film transistor of claim 1, wherein the source region overlaps the gate electrode.

5. (original) The thin film transistor of claim 1, wherein the source region comprises two strip regions, each of the two strip regions adjacent to each longitude of the drain region.

6. (original) The thin film transistor of claim 1, wherein the shape of the notch of the gate electrode is a triangle, a quadrilateral or a non-regular shape.

7. (original) A pixel structure, comprising:

a scan line, formed on a substrate;

a gate electrode, formed on the substrate and electrically connected to the scan line, wherein the gate electrode has at least one notch;

a gate dielectric layer, formed over the substrate, covering the scan line and the gate electrode;

a channel layer, formed over the gate dielectric layer and located over the gate electrode;

a source region, formed on the channel layer, wherein the source region is over a region outside the notch of the gate electrode and the source region overlaps a portion of the gate electrode;

a drain region, formed over the channel layer exposed by the source region, wherein the drain region is over the notch of the gate electrode and the drain region overlaps a portion of the gate electrode at the edge of the notch;

a data line, formed on the gate dielectric layer, wherein the data line is electrically connected to the source region;

a protection layer, formed over the substrate, covering the gate electrode, the gate dielectric layer, the channel layer, the source region, the drain region, the scan line and the data line;

a contact, formed within the protection layer and electrically connected to the drain region; and

a pixel electrode, formed on the protection layer, the pixel electrode electrically connected to the drain region through the contact.

8. (original) The pixel structure of claim 7, further comprising an etch stop layer formed between the channel layer and the source and drain regions.

9. (original) The pixel structure of claim 7, further comprising an ohmic-contact layer formed between the channel layer and the source and drain regions.

10. (original) The pixel structure of claim 7, wherein the source region overlaps the gate electrode.

11. (original) The pixel structure of claim 7, wherein the source region comprises two strip regions, each of the two strip regions adjacent to each longitude of the drain region.

12. (original) The pixel structure of claim 11, wherein the source region further extends over the gate dielectric layer formed on the scan line.

13. (original) The pixel structure of claim 7, wherein the shape of the notch of the gate electrode is a triangle, a quadrilateral or a non-regular shape.

Claims 14 –19 (cancelled)